Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-6. (canceled)

Claim 7. (currently amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer ~~therebetween~~ between layers of said polyimide tape;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said copper foil layer traverses said wiring layer from a first bonding pad on said wiring layer to a second bonding pad on said wiring layer,

wherein said copper foil is connected to said substrate

through a first bonding wire only at said first bonding pad, and

wherein said copper foil is connected to said second semiconductor chip through a second bonding wire only at said second bonding pad.

Claim 8. (currently amended) The semiconductor device according to claim 7, wherein,

~~a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip;~~

~~a second~~ said first bonding wire connects one of said plural bonding pads on said substrate to ~~one of said plural bonding pads~~ said first bonding pad on said wiring layer; [[and]]

~~a third~~ said second bonding wire connects said ~~one of said plural bonding pads~~ second bonding pad on said wiring layer to one of said plural bonding pads on said second semiconductor chip; and ~~substrate~~

a third bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip.

Claim 9. (canceled)

Claim 10. (previously presented) The semiconductor device according to claim 7, further comprising a via hole in said

wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

Claim 11. (previously presented) The semiconductor device according to claim 9, further comprising a via hole in said wiring layer, said via hole having a contact for connecting yet another one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

Claim 12. (currently amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a conductor laminated between polyimide layers;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said second semiconductor chip is mounted on

said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material,

wherein said conductor inside said wiring layer is outside said second semiconductor chip and is connected to a first bonding pad on said wiring layer nearest a first edge of said second semiconductor chip and is connected to a second bonding pad on said wiring layer nearest a second edge of said second semiconductor chip,

wherein said conductor is connected to said substrate only at said first bonding pad, and

wherein said conductor is connected to said second semiconductor chip only at said second bonding pad.

Claim 13. (canceled)

Claim 14. (currently amended) The semiconductor device according to claim 12, wherein

a first bonding wire connects one of said plural bonding pads on said substrate to one of said plural bonding pads on said first semiconductor chip;

a second bonding wire connects one of said plural bonding pads on said substrate to ~~one of said plural bonding pads~~ to said first bonding pad on said wiring layer; and

a third bonding wire connects ~~another one of said plural bonding pads~~ said second bonding pad on said wiring layer to one of said plural bonding pads on said second semiconductor ~~substrate~~ chip, said second and third bonding wire being electrically connected through said conductor.

Claim 15. (previously presented) The semiconductor device according to claim 12, wherein said wiring layer comprises a lamination of polyimide layer and an aluminum layer.

Claim 16. (previously presented) The semiconductor device according to claim 12, further comprising a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

Claim 17. (currently amended) A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including an inner layer conductor traversing said wiring layer;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips; and

a plurality of bonding wires for connecting said plural bonding pads to each other,

wherein said inner layer conductor traverses said wiring layer from a first bonding pad on said wiring layer to a second bonding pad on said wiring layer,

wherein said inner layer conductor is connected to said substrate only at said first bonding pad, and

wherein said inner layer conductor is connected to said second semiconductor chip only at said second bonding pad.

Claim 18. (previously presented) The semiconductor device according to claim 17, further comprising a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip.

Claim 19. (canceled)

Claim 20. (currently amended): A semiconductor device comprising:

a substrate;

a first semiconductor chip on said substrate;

a second semiconductor chip overlying said first semiconductor chip;

a wiring layer between said first and second semiconductor chips, said wiring layer including a polyimide tape having a copper foil layer ~~therebetween~~ between layers of said polyimide tape;

a plurality of bonding pads on said wiring layer, said substrate and said first and second semiconductor chips;

a plurality of bonding wires for connecting said plural bonding pads to each other; and

a via hole in said wiring layer, said via hole having a contact for connecting one of said plural bonding pads on the wiring layer to one of said plural bonding pads on said first semiconductor chip,

wherein said second semiconductor chip is mounted on said wiring layer by an adhesive material and said wiring layer is provided on said first semiconductor chip without using an adhesive material,

wherein said copper foil layer is outside said second semiconductor chip and is connected to a first bonding pad on said wiring layer nearest a first edge of said second semiconductor chip and is connected to a second bonding pad on said wiring layer nearest a second edge of said second semiconductor chip,

wherein said copper foil layer is connected to said

substrate only at said first bonding pad, and

wherein said copper foil layer is connected to said second semiconductor chip only at said second bonding pad.

Claim 21. (canceled)

Claim 22. (new) The semiconductor device as claimed in claim 12, wherein the second edge is opposite the first edge.

Claim 23. (new) The semiconductor device as claimed in claim 17, wherein said wiring layer is integral with said first semiconductor chip.

Claim 24. (new) The semiconductor device as claimed in claim 20, wherein the second edge is opposite the first edge.